REMARKS

Reconsideration of this application, as presently amended, is respectfully requested. Claims 1, 2, 7, 8, 13 and 15 are now pending in this application, new claim 15 having been added by the present Amendment. Claims 3 – 6, 9 -12 and 14 have been canceled. Claims 1, 2, 8 and 13 stand rejected. Claim 7 has been allowed. No new matter has been added. The rejections set forth in the Office Action are respectfully traversed below.

Claim Rejections – 35 U.S.C. §102

Claims 1-2, 8 and 13-14 stand rejected under 35 U.S.C. §102(b) as being anticipated by **Freeman** (Re 34,363). It is noted that claim 14 was cancelled in the Amendment filed January 8, 2004. Therefore, the rejection of claim 14 is disregarded. For the reasons set forth in detail below, this rejection, to the extent it is considered to apply to the amended claims, is respectfully traversed.

Claims 1 and 8

Claim 1 has been amended to clarify that the transmission section *selects between* outputting of the inverted first input signal and the inverted second input signal in response to an externally controllable selection signal and an inverted signal of the selection signal.

As set forth on pages 2 and 3, Item 4 of the Office Action, the Examiner considers the inverters 21 and 22, shown in Figure 2 of **Freeman**, to correspond to the claimed first and second inversion sections, respectively. The Examiner interprets the lines and pass transistors

(e.g., 29c, 29d) that connect the inverters 21, 22 to the OR gate 23 and the AND gate 25 to correspond to the claimed transmission section.

As shown in Figure 2 and described in column 4, line 40 – column 5, line 8 of **Freeman**, the outputs of the inverters 21 and 22 are selectively connected to either the OR gate 23 or the AND gate 25 depending on the ON/OFF state of the various pass transistors (e.g., 29c, 29d). The ON/OFF state of the pass transistors is controlled by configuration control signals C0, /C0, C1, /C1, C2, /C2, C3, /C3.

The configuration control signals C0, /C0, C1, /C1, C2, /C2, C3, /C3 are supplied to the pass transistors to select whether an inverted or non-inverted form of respective input signals A and B are supplied to the OR gate 23 and the AND gate 25. For example, the pair of control signals C0, /C0 is used to select whether an inverted or non-inverted form of input signal B is supplied to AND gate 25. Specifically, if the signal C0 is high (and the corresponding signal /C0 is low), then the non-inverted signal B is supplied to the AND gate 25. Conversely, if the signal C0 is low (and the corresponding signal /C0 is high), then the inverted signal /B is supplied to the AND gate 25. The other pairs of control signals (C1, /C1, etc.) function similarly in that they select either the inverted or non-inverted signals A, /A and B, /B for transmission to the AND gate 25 and OR gate 23.

Thus, **Freeman** teaches that a pair of configuration control signals (C0, /C0, etc.) and corresponding pair of pass transistors is *capable of selecting the output of only one of the inverters* 21, 22. In other words, *two pairs of configuration control signals* (e.g., C0, /C0 and C1, /C1) and corresponding pass transistors are required to select *between* outputting a signal from

the inverter 21 and a signal from the inverter 22. For example, to select between outputting a signal from inverter 21 and inverter 22 to the OR gate 23, it is necessary to use configuration control signals C2, /C2, C3, /C3.

Freeman does not disclose or suggest a transmission section, as recited in claim 1, that *selects between outputting of the inverted first input signal and the inverted second input signal in response to an externally controllable selection signal and an inverted signal of the selection signal.*

In contrast, according to **Freeman**, two selection signals (e.g., C0, /C0) can *only* select between outputting an inverted signal (e.g., /A) and a non-inverted signal (e.g., A), and can *not* select between outputting of two inverted signals. As discussed above, unlike the invention recited in claim 1, the **Freeman** circuit requires four selection signals (e.g., C0, /C0, C1, /C1) to select between outputting of inverted signals /A and /B.

Claim 8

Claim 8 depends from claim 1 and is allowable for all the reasons set forth above with respect to claim 1. Moreover, claim 8 includes additional features not disclosed or suggested by the **Freeman** reference.

The Office Action asserts that Figure 2 of **Freeman** discloses the *first switching section* recited in claim 8 as the lines connected to the pass transistors controlled by configuration control signals C2, /C2 and which feed the signals A, /A to OR gate 23. The Office Action further asserts that Figure 2 of **Freeman** discloses the *second switching section* recited in claim 8

as the lines connected to the pass transistors controlled by configuration control signals C3, /C3 and which feed the signals B, /B to OR gate 23. See Office Action page 3, lines 14-22.

However, claim 8 clearly recites that the first and second switching sections are *provided on the input side* of the first and second inversion sections, respectively. In contrast, **Freeman** discloses that the lines connected to the pass transistors controlled by C2, /C2 and C3, /C3 are *not on the input side* of the inverters 21, 22, and are clearly *on the output side* of the inverters 21, 22.

Claim 2

Independent claim 2 has been amended in a manner similar to the amendment of claim 1, to clarify that the *first outputting section* and the *second outputting section* respectively select between the output of the first inversion section and the second inversion section in response to an externally controllable selection signal and an inverted signal of the selection signal.

In the rejection of independent claim 2, set forth on page 3, lines 3-13 of the Office Action, the Examiner also relies on Figure 2 of **Freeman** and asserts that the AND gate 25 corresponds to the claimed *first outputting section*, and that the signals C1 and /A correspond to the *externally controllable first selection signal* and the *inverted signal of the first selection signal*, respectively.

Similarly, the Office Action asserts that the AND gate 24 corresponds to the claimed *second outputting section*, and that the signals /B and C3 correspond to the *externally controllable second selection signal* and the *inverted signal of the second selection signal*, respectively.

First, it is noted that **Freeman** does not disclose or suggest that the respective pairs of signals C1, /A and /B, C3, which the Examiner asserts correspond to the claimed *selection signals and inverted signals of the selection signals*, are inverted signals with respect to each other. Specifically, /A is not an inverted signal of C1 (and vice versa). Similarly, C3 is not an inverted signal of /B (and vice versa).

Further, **Freeman** does not disclose or suggest the claimed first outputting section and the claimed second outputting section for respectively *selecting between output of the first inversion section and second inversion section in response to an externally controllable selection signal and an inverted signal of the selection signal.* In contrast, the control signals C0, /C0, etc. disclosed by **Freeman**, which are inverted with respect to each other, function to select a *single* inverted or non-inverted output, and do *not* select between the outputs of two inversion sections, as presently recited in claim 2.

Claim 13

With respect to independent claim 13, on page 4, lines 3-5 of the Office Action, the Examiner asserts that the inverter 21 shown in Figure 2 of **Freeman** corresponds to the claimed *first inversion section* and is "essentially composed of transistor circuits... each of [the] transistor circuits having a first input signal terminal (input of [inverter] 21) for the first input signal (A)." Similarly, on page 4, lines 9-11 of the Office Action, the Examiner asserts that the inverter 22 shown in Figure 2 of **Freeman** corresponds to the claimed *second inversion section* and is "essentially composed of transistor circuits... each of [the] transistor circuits having a second input signal terminal (input to [inverter] 22) for the second input signal (B)."

However, the inverters 21 and 22 shown in Figure 2 of **Freeman** are illustrated using the standard logic symbol for an inverter. The **Freeman** reference goes into no detail about the specific circuit structure of the inverters 21, 22, and does not disclose or suggest the claimed *first (and second) inversion section including transistor circuits, each transistor circuit having a first (second) input signal terminal for the first(second) input signal.*

In the absence of any description in **Freeman** concerning the transistor circuit structure of the inverters 21, 22, the Examiner has not properly rejected claim 13 under §102 because Freeman does not disclose each and every element in claim 13.

In view of the above amendments and remarks, reconsideration and withdrawal of the rejection of claims 1, 2, 8, and 13 under 35 U.S.C. §102(b) are respectfully requested.

New Claim 15

New claim 15 has been added. New claim 15 recites the invention similarly to claim 1 and more particularly defines the selection of the first and second inverted signals. None of the cited prior art disclose or suggest a selector as recited in claim 15.

CONCLUSION

For the reasons set forth in detail above, it is respectfully submitted that all pending claims are in condition for allowance. An indication of allowability of all pending claims is respectfully requested.

If the Examiner believes that there are any issues remaining to be resolved in this application, the Examiner is invited to contact the undersigned attorney at the telephone number indicated below to arrange for an interview to expedite and complete prosecution of this case.

In the event that any fees are due in connection with the filing of this paper, please charge any fees to Deposit Account No. 50-2866.

Respectfully submitted,

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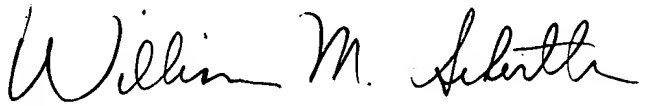

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